L	Hits	Search Text	DB	Time stamp
Number 1	165	712/206.ccls.	USPAT	2004/11/03
2	292	712/208.ccls.	USPAT	09:45 2004/11/03
				09:45
3	218	712/209.ccls.	USPAT ·	2004/11/03 09:45
4	212	712/213.ccls.	USPAT	2004/11/03
5	351	712/210.ccls.	USPAT	2004/11/03
6	47	(width near4 bits) with instruction with	USPAT; EPO; JPO	2004/11/03
7	89	(width size length) with instruction with	USPAT;	2004/11/03
8	6	(signal indicat\$4) with bit with decoder bits with instruction with size with	EPO; JPO USPAT;	09:45 2004/11/03
9	32	indicat\$4 with width emulation near3 ("instruction register"	EPO; JPO USPAT;	09:45 2004/11/03
10	126	IR) (decod\$4 near4 priority) with instruction	EPO; JPO USPAT;	09:45 2004/11/03
12	7	(emulation near3 ("instruction register"	EPO; JPO USPAT;	09:45 2004/11/03
	,	IR)) and ((decod\$4 near4 priority) with instruction)	EPO; JPO	09:45
13	50	decoder with width with bit with instruction	USPAT; EPO; JPO	2004/11/03
15	99	multiplexor with decoder with instruction	USPAT; EPO; JPO	2004/11/03
11	9	(US-6182280-\$ or US-6110225-\$ or	USPAT	2004/11/03
		US-6449712-\$ or US-5941980-\$ or US-5931944-\$ or US-5920713-\$ or		09:46
		US-5832258-\$ or US-5809272-\$ or US-6260134-\$ or US-5845102-\$).did.		
16	20	multiplexor with decoder with instruction with input	USPAT; EPO; JPO	2004/11/03
17	180	instruction with cache with bypass	USPAT; EPO; JPO	2004/11/03
14	19	speculative with ("instruction register")	USPAT	2004/11/03
18	123	instruction with cache with bypass	USPAT; EPO; JPO	2004/11/03
19	5	("instruction cache" with bypass) same decoder	USPAT; EPO; JPO	2004/11/03
20	13	(instruction with cache with bypass) same	USPAT;	2004/11/03
23	112	decoder instruction with cache with bypass	EPO; JPO USPAT	2004/11/03
21	5	("instruction cache" with bypass) same	USPAT	09:46
22	13	decoder (instruction with cache with bypass) same	USPAT	09:46 2004/11/03
_	13074	decoder width near4 bits	USPAT	09:46 2003/09/24
_	527	(width near4 bits) with instruction	USPAT	14:12 2003/09/24
_	39	(width near4 bits) with instruction with	USPAT	16:09 2004/04/13
_	171	size bits with instruction with size with	USPAT	16:16 2003/09/24
_	5	indicat\$4 bits with instruction with size with	USPAT	14:22 2004/04/13
_	795	indicat\$4 with width plurality with source with decoder	USPAT	16:16 2003/09/24
	59		USPAT	15:18 2004/04/13
				16:16
_	3	(plurality near3 source near3 decoder) with instruction	USPAT	2003/09/24
-	86	•	USPAT	2004/04/13 16:16
_	0	(width near4 bits) with instruction with decoder with (mux multiplexor)	USPAT	2003/09/24 16:09

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-	1	(width near4 bits) same (instruction with	USPAT	2003/09/24
	_	decoder with (mux multiplexor))		16:11
-	2	(width near4 bits) same (instruction with	USPAT	2003/09/24
	2.4	decoder) same (mux multiplexor)		16:12
-	34	(width size length) same (instruction	USPAT	2003/09/24
	2002	with decoder) same (mux multiplexor)	USPAT	16:16 2003/09/24
-	2983	(width size length) with instruction with	USPAI	16:17
	746	(signal indicat\$4) (width size length) with instruction with	USPAT	2003/09/24
-	740	(signal indicat\$4) with bit	USFAI	16:17
_	74	(width size length) with instruction with	USPAT	2004/04/13
-	/ 3	(signal indicat\$4) with bit with decoder	OSIAI	16:16
_	0	(width size length) with instruction with	USPAT	2003/09/24
		(signal indicat\$4) with bit with decoder		16:17
	· '	with (multiplexor mux)		
i -	1	((width size length) with instruction	USPAT	2003/09/24
1		with (signal indicat\$4) with bit with		16:17
		decoder) same (multiplexor mux)		
-	6	5809272.URPN.	USPAT	2003/09/24
	_			17:11
-	2	1 , , , , , , , , , , , , , , , , , , ,	USPAT	2003/09/25
		US-6449712-\$ or US-5941980-\$ or		12:05
]		US-5931944-\$ or US-5920713-\$ or		
		US-5832258-\$ or US-5809272-\$ or		
		US-6260134-\$ or US-5845102-\$).did.) and dsp		
	103	dsp (decod\$4 near4 priority) with instruction	USPAT	2004/04/13
"	103	(accords hears priority) with instruction	704414	16:16
_	8	((decod\$4 near4 priority) with	USPAT	2003/09/26
		instruction) and dsp		16:25
-	3	((decod\$4 near4 priority) with	US-PGPUB	2003/09/26
		instruction) and dsp		16:25
-	17	emulation near3 "instruction register"	USPAT	2004/04/13
	_	2 (8) 5 5 6 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7	TTCD N CO	16:16 2004/04/13
-	7	<pre>(emulation near3 ("instruction register" IR)) and ((decod\$4 near4 priority) with</pre>	USPAT	16:15
		instruction)		10.15
1_	l .	instruction	USPAT	2003/09/26
-		emulation instruction register	051111	16:33
_	l 0	"emulation ir"	USPAT	2003/09/26
				16:33
-	26	emulation near3 ("instruction register"	USPAT	2004/04/13
		IR)		16:16
-	2367	(plural\$4 multiple) with ("instruction	USPAT	2003/09/26
	700	register" IR)	IICDAM	16:44 2003/09/26
_	708	(plural\$4 multiple) with ("instruction register")	USPAT	16:44
_	99	instruction with decoder with multiplexor	USPAT;	2004/10/29
			EPO; JPO	16:42
_	68	plurality near3 source near3 decoder	USPAT;	2004/10/29
			EPO; JPO	16:42
-	99	instruction with decoder with multiplexor	USPAT;	2004/10/29
			EPO; JPO	16:42
-	287	(plural\$4 multiple) near3 ("instruction	USPAT	2004/10/29
		register")	IICD2M	16:42
-	125	(decod\$4 near4 priority) with instruction	USPAT; EPO; JPO	2004/10/29 16:42
1_	20	emulation near3 "instruction register"	USPAT;	2004/10/29
	20	emuracion hears instruction register	EPO; JPO	16:42
-	2	((plural\$4 multiple) near3 ("instruction	USPAT	2004/10/29
	1	register")).ti.		16:42
-	1	5721855.pn.	USPAT	2004/10/29
				17:02
-	0	(multiplexor with decoder with	USPAT	2004/10/29
		instruction) and (decoder with width with		17:02
		bit)		2004/10/00
-	37		USPAT	2004/10/29
1_	99	instruction multipleyor with decoder with instruction	USPAT	18:14 2004/10/29
-	99	multiplexor with decoder with instruction	USFAI	18:14
_	20	multiplexor with decoder with instruction	USPAT	2004/10/29
		with input		18:14
L		1.27 = 525		

-	169	instruction w	ith cache	with bypass	USPAT	2004/10/29	Ī
						18:14	ı